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62-18714

METHOD OF FORMING ALIGNMENT MARK

(Araimento Maku no Keisei Hoho)

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UNITED STATES PATENT AND TRADEMARK OFFICE

Washington, D. C. March 2002

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Applicant	:	Nippon Telegram and Telephone Corp. (NTT)
IPC	:	H 01 L 21/30 C 23 F 4/00 H 01 L 21/302
Application Date	:	July 18, 1985
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Foreign Language Title	:	Araimento Maku no Keisei Hoho
English Title	:	METHOD OF FORMING ALIGNMENT MARK

SPECIFICATION

I. Title of the Invention

Method of Forming Alignment Mark

II. Claims

1. In a method of forming alignment mark which comprises portions having a high reflectivity to light and portions having a low reflectivity to light, detects reflected lights reflected by these two portions and takes an alignment control of a substrate where these two portions are formed,

a member having corrosion resistance is arranged by dry etching method using a plasma only in the portions which should take said high reflectivity and then etched by said dry etching method to form very fine roughness group in the portions which should take said low reflectivity of said alignment mark.

III. Detailed Description of the Invention

[Technical Field of the Invention]

This invention relates to a method of forming an alignment mark arranged on a substrate to be exposed in a manufacturing process of semiconductor integration circuit.

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[1]Numbers near the margin indicate pagination in the foreign text.

[Technical Background of the Invention and Its Problems]

The microfining of dimensions of circuit patterns has been pursued with the high integration of recent semiconductor integrated circuits. Therefore, not only a high resolution but also a high alignment accuracy have increasingly been required in an exposure device for transferring a circuit pattern to a semiconductor substrate.

The alignment of a mask for exposure and a substrate to be exposed in a conventional exposure device detects reflected lights obtained by irradiating a light to both alignment marks and is performed by a technique for combining relative positions of the both.

For example, Japan Tokkyo Appl. 55-034369 is given as such an alignment device. The detection principle of alignment marks is illustrated by Fig. 3. In Fig. 3(a), **1** is an alignment mark of mask, **2-a**, **2-b** are high reflecting portions for an illuminating light **7**, **3** is a transmission portion, **4** is an alignment mark of wafer arranged on a substrate **10**, **5** is a high reflecting portion, and **6-a** and **6b** are low reflecting portions.If reflected lights **8-a**,

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8-b, **9** obtained by irradiating the illuminating light **7** onto the both alignment marks are detected by a light receiver such as ITV camera, CCD camera, etc., electric signals as shown in Fig. 3(b) are obtained. **11-a**, **11-b** are signals corresponding to the mask alignment mark, and **12** is a signal corresponding to the wafer

alignment mark. The relative positional relation of said mask and wafer alignment marks are detected from these electric signals, and alignment devices of mask and wafer are controlled so that the relation of the both satisfies a predetermined value. In such alignment devices, it is required that the SN ratio of detected signals of said mask alignment mark and said wafer alignment mark be increased to enhance the alignment accuracy. Namely, it is required that the optical contrast of said alignment marks be high. Particularly, reflected lights from the low reflecting portions **6-a, 6-b** of said a wafer alignment mark become **13-a** and **13-b**, therefore it is important to suppress them to as small values as possible. For this reason, it is desired to optimize the mark shape.

Such a wafer alignment mark with a high contrast and manufacturing method thereof have been disclosed in Japan Kokai S58-90728. The manufacturing method is illustrated by Fig. 4. First, a mask material layer **14** of SiO_2, Si_3O_4, etc. is formed on a semiconductor substrate **10** of Fig. 4(a). Next, as shown in Fig. 4(b), a photoresist **15** is coated on the mask material layer **14**, many alignment space resist patterns **16-a, 16-b** and a linear resist pattern **17** are formed by photolithography so that they become equal to sizes of the low reflecting portions **6-a, 6-b** and the high reflecting portion **5** of Fig.3, respectively. Subsequently, as shown in Fig. 4(c), many line-and-space mask material layer patterns **18-a, 18-b** and a straight line mask material layer pattern **19** corresponding to the

photoresist patterns are formed on the mask material layer **14** by etching the photoresist patterns into a mask for the mask material layer **14** and then the photoresist **15** is removed. Next, as shown in Fig. 4(d), a plasma etching treatment is made as an isotropic etching treatment for the semiconductor substrate **10** with the patterns **18-a**, **18-b** and **19** formed on the mask material layer **14** as mask, regions **20-a**, **20-b** composed of array of many very fine pits having a circular arc cross-section, subsequently the etching mask material layer **14** is removed from the semiconductor substrate **10** to obtain an objective alignment mark of Fig. 4(e).

This alignment mark reduces the reflectivity for an illuminating light because portions corresponding to the low reflecting portions **6-a** and **6-b** of Fig. 3 become many very fine circular arc patterns **21-a**, **21-b**, while the contrast of said alignment mark increases because portions corresponding to the high reflecting portion **5** becomes a smooth surface.

In the above conventional method of forming said alignment mark, however, there was such a problem that process steps became complicated because special alignment space resist patterns **16-a**, **16-b** had to be formed after the mask material layer **14** of Fig. 4 was formed. Moreover, the etching had to be stopped under optimum conditions to obtain the circular arc patterns **21-a**, **21-b** of Fig. 4(e), thus the final judgment was difficult. If this etching became

under or over, there was a problem of becoming defects because the contrast of alignment mark reduces. Thus, there was a drawback that the yield did not increase because no margins exist under etching conditions.

[Purpose of the Invention]

This invention consists in providing a forming method of alignment mark arranged on a substrate to be exposed which has a high optical contrast, simple formation steps and a high yield of said alignment mark.

[Outline of the Invention]

The characteristics of this invention consist in that an alignment mark can be formed by once dry etching without forming line-and-space resist patterns for forming an etching mark mate-

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rial layer and a very fine roughness group needed in the conventional technique. It is different from the conventional mark forming technique in that a step of forming an etching mark material layer, a dry etching step corresponding thereto and a step of removing the mark material layer are excluded.

[Actual Examples of the Invention]

This invention is a method of forming alignment mark which comprises portions having a high reflectivity to light and portion having a low reflectivity to light, detects reflected lights reflected by these two portions and takes an alignment control of

a substrate where these two portions are formed,

a member having corrosion resistance is arranged by dry etching method using a plasma only in the portion which should take said high reflectivity, etched by said dry etching method and a very fine roughness group is formed in the portion which should take said low reflectivity of said alignment mark, and this invention is illustrated in detail while seeing the following drawings.

Fig. 1 is a schematic diagram for illustrating Actual Example 1. A wafer of plane orientation (100) being a silicon single crystal is used in a semiconductor substrate **10** of Fig. 1(a), a resist **15** having corrosion resistance is coated on the surface thereof by dry etching, a resist pattern **24** and resist-free portions **23-a, 23-b** of an alignment mark pattern are formed by a well-known method. The resist pattern **24** is formed so as become equal to the size of a high reflecting portion **5** of said alignment mark of Fig. 3 and the resist-free portions **23-a, 23-b** are formed so as become equal to the size of low reflecting portions **6-a, 6-b** of said alignment mark of Fig. 3, respectively. Next, if a dry etching using a high-frequency glow discharge with CCl_2F_2 as gas is applied, the resist-free portions **23-a, 23-b** of Fig. 1(a) are filled up by a very fine quadrangular protrusion group as shown by **25-a, 25-b** of Fig. 1(b). This dry etching method and the shape have been disclosed in K. Hirata et al, "Dry Etching Technology for 1 μm VLSI Fabrication", *IEEEED*, **28** (11), 1323 (1981). Its dimensions become about 1 μm in

base and 1 - 2 μm in height. Subsequently, if the resist **15** of Fig. 1(b) is removed by a well-known method, it becomes a shape shown in Fig. 1(c). The lower part of said resist pattern **26** is a flat plane as it is, but the surface of said protrusion group of etching portion becomes a rough surface and therefore becomes a surface which has extremely low reflectivity to an illuminating light and is near to a black body. Accordingly, if this alignment mark is optically detected, an extremely high contrast is obtained.

Thus, this invention enables to form an alignment mark which is extremely simple and has an extremely high contrast as compared to the conventional method shown in Fig. 4. Moreover, it also enables to obtain an alignment mark in a high yield and also sharply improve the productivity because etching margins are larger than in the conventional method.

[Actual Example 2]

Fig. 2 is a schematic diagram for illustrating another actual example. A resist **15** is coated and a resist pattern **24** and resist-free portions **23-a, 23-b** of an alignment mark pattern are similarly formed by a well-known method on a wafer with a Mo film **27** formed on a substrate **10**. Next, if a dry etching using a high-frequency glow discharge with a mixed gas of CF_4 and O_2 is applied, roughness groups **28-a, 28b** with a forest of very fine columar crystals are obtained as shown in Fig. 2(b). This dry etching method and the shape have been disclosed in Oda et al, "Crystal structure of Mo

Film and Plasma Etching Characteristics", *Preprints of 2nd Dry Process Symposium*, 87 (1980). Its dimensions become about 1 μm in base and 1 - 2 μm in height. Subsequently, if the resist **15** is removed by a well-known method, it becomes Fig. 1(c). The lower part of said resist pattern **29** is a flat plane as it is, but the surface of said roughness groups **28-a**, **28b** of etched portion becomes a rough surface, therefore it becomes a surface which has extremely low reflectivity to an illuminating light and is near to a black body.

Thus, this invention enables to form an alignment mark which is extremely simple and has an extremely high contrast for a metal-

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film like Mo.

This invention is not restricted to the above actual examples, and its application range is extremely wide because the surface conditions of various materials can be optically made into very fine rough shape with a low reflectivity if a well-known dry etching method is applied.

[Effects of the Invention]

As described above, this invention enables to sharply improve the contrast of an alignment mark arranged on a substrate to be exposed for an illuminating light, and this forming method has advantages that it is extremely simple and gives an extremely high yield.

IV. Brief Description of the Drawings

Fig. 1 is sectional views showing one actual example of this invention, Fig. 2 is sectional views showing another actual example of this invention, Fig. 3 is drawings illustrating a detection principle of alignment marks, and Fig. 4 is sectional views illustrating a forming method of conventional alignment marks.

1 ... alignment mark of mask

2 ... high reflecting portion

3 ... transmission portion

4 ... alignment mark of wafer

5 ... high reflecting portion

6 ... low reflecting portion

7 ... illuminating light

8 ... reflected light from mask mark

9 ... reflected light from wafer mark

10 ... substrate

11 ... detecting signal of mask mark

12 ... detecting signal of wafer mark

13 ... background

14 ... mask material layer

15 ... resist

16 ... line-and-space resist pattern

17 ... linear resist pattern

18 ... line-and-space mask material layer pattern

19 ... linear mask material layer pattern

20 ... region composed of array of many very fine pits having circular arc cross-section

21 ... circular arc pattern

22 ... smooth surface

23 ... resist-free portion of alignment mark pattern

24 ... resist pattern of alignment mark pattern

25 ... very fine quadrangular protrusion group

26 ... lower part of resist pattern

27 ... Mo film

28 ... roughness group with a forest of very fine columar crystals

29 ... lower part of resist pattern

Fig. 1

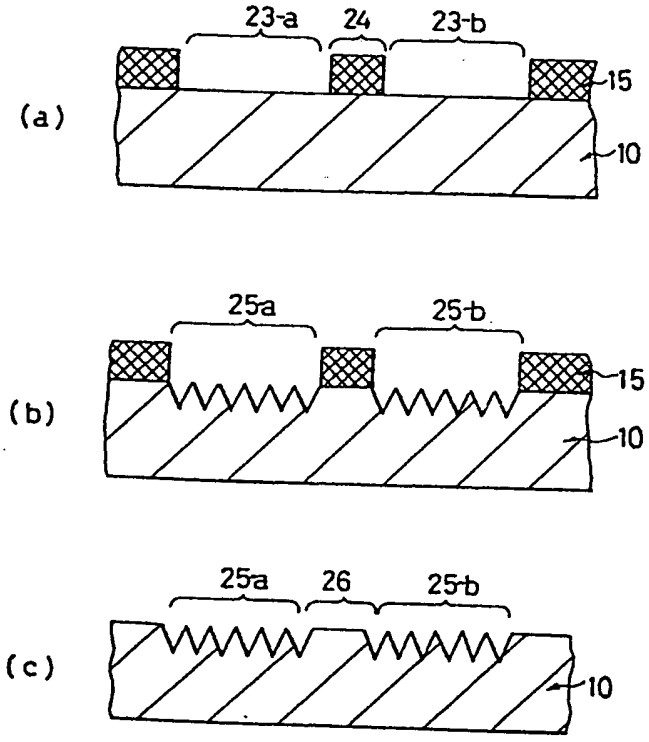

(a)
23-a
24
23-b
15
10
(b)
25a
25-b
15
10
(c)
25a
26
25-b
10

Fig. 2

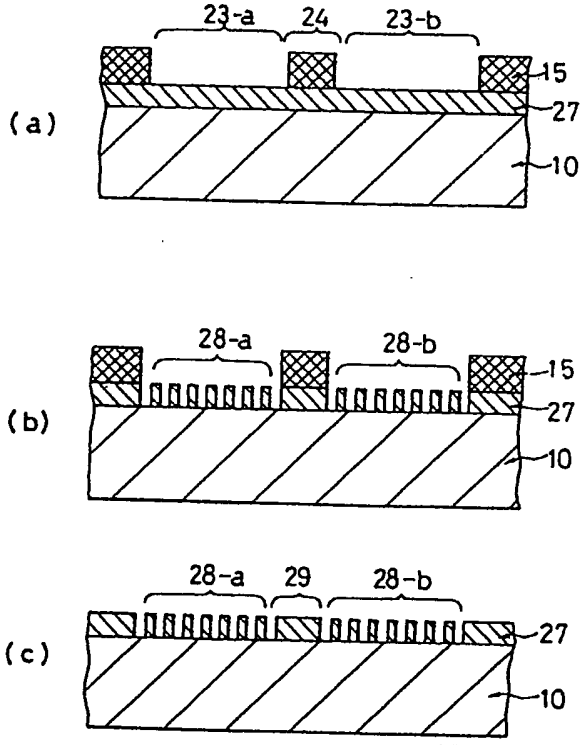

(a)
23-a
24
23-b
15
27
10
(b)
28-a
28-b
15
27
10
(c)
28-a
29
28-b
27
10

Fig. 3

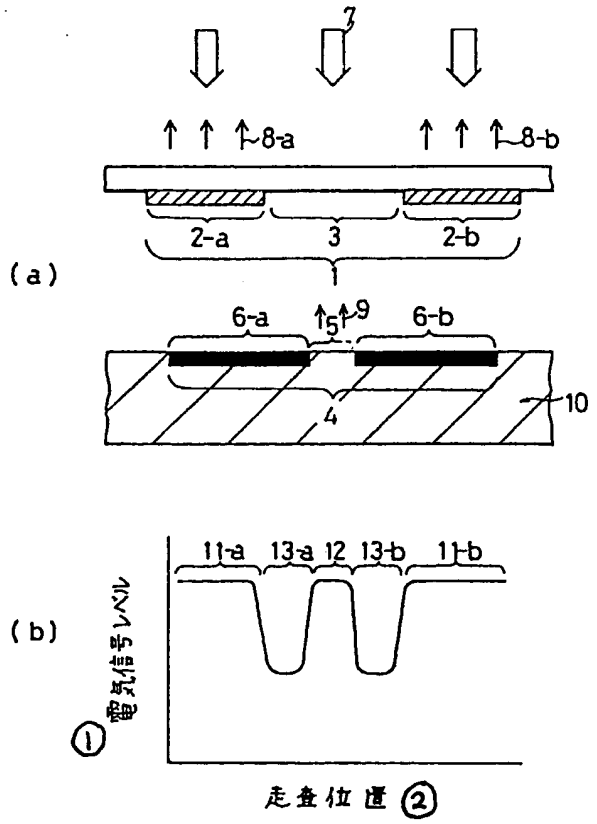
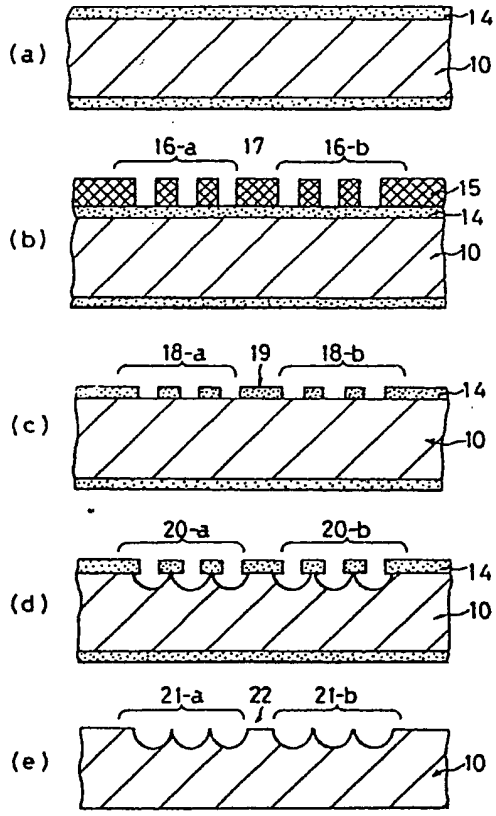


Fig. 4



(1) Electric signal level

(2) Scanning position